CLAIMS

What is claimed is:

1. A method for forming at least one non-volatile memory cell, comprising:
forming a first oxide layer, an electron trapping layer, a second oxide layer, a first electrically conductive layer, and a dielectric layer on a surface of a substrate in that order;
patterning the dielectric layer and the first electrically conductive layer, thereby forming at least one component stack;
depositing a third oxide layer over and beside the at least one component stack;
removing a portion of an upper section of the third oxide layer opposite the second oxide layer such that an upper portion of the dielectric layer is exposed through the third oxide layer;
removing the dielectric layer and a remaining portion of the upper section of the third oxide layer such that an elevation of an upper surface of the third oxide layer above the surface of the substrate is substantially equal to an elevation of an upper surface of the patterned first electrically conductive layer; and
forming a second electrically conductive layer over upper surfaces of the patterned first electrically conductive layer and the third oxide layer.

2. The method as recited in claim 1, wherein the depositing of a third oxide layer comprises depositing a third oxide layer over and beside the component stack via a high density plasma chemical vapor deposition (HDP CVD) process.

3. The method as recited in claim 1, wherein the depositing of a third oxide layer is carried out at a temperature lower than a temperature required to thermally grow the third oxide layer.

4. The method as recited in claim 1, wherein the depositing of a third oxide layer is carried out such that the third oxide layer has a thickness between about 1200 Angstroms and approximately 1400 Angstroms.

5. The method as recited in claim 1, wherein the removing of a portion of an upper section of the third oxide layer comprises dipping the portion of the upper section in an etchant solution.

6. The method as recited in claim 1, wherein the electron trapping layer comprises silicon nitride.

7. The method as recited in claim 1, wherein the first electrically conductive layer comprises doped polysilicon.

8. The method as recited in claim 1, wherein the dielectric layer comprises silicon nitride.

9. The method as recited in claim 1, wherein the second electrically conductive layer comprises doped polysilicon.

10. The method as recited in claim 1, wherein:

the patterning further comprises patterning the second oxide layer, the electron trapping layer, and the first oxide layer, to thereby form the at least one component stack; and

the depositing of a third oxide layer over and beside the at least one component stack is preceded by forming an oxide layer beside the component stack.

11. A semiconductor structure formed using the method set forth in claim 10.

12. A semiconductor structure formed using the method set forth in claim 1.

13. A semiconductor structure formed using the method set forth in claim 3.

14. A method for forming at least one non-volatile memory cell, comprising:
forming a first oxide layer, a first nitride layer, a second oxide layer, a first electrically conductive layer, and a second nitride layer on a surface of a substrate in that order;
patterning the second nitride layer and the first electrically conductive layer, thereby forming at least one component stack;
using the at least one component stack as a doping mask to selectively introduce dopant atoms into the surface of the substrate, thereby forming a bit line in the substrate adjacent to the at least one component stack;
depositing a third oxide layer over and beside the component stack;
removing a portion of an upper section of the third oxide layer opposite the second oxide layer such that an upper portion of the second nitride layer is exposed through the third oxide layer;
removing the second nitride layer and a remaining portion of the upper section of the third oxide layer such that an elevation of an upper surface of the third oxide layer above the surface of a substrate is substantially equal to an elevation of an upper surface of the patterned first electrically conductive layer; and
forming a second electrically conductive layer over upper surfaces of the patterned first electrically conductive layer and the third oxide layer.

15. The method as recited in claim 14, wherein the depositing of a third oxide layer comprises depositing a third oxide layer over and beside the component stack via a high density plasma chemical vapor deposition (HDP CVD) process.

16. The method as recited in claim 14, wherein the depositing of a third oxide layer is carried out at a temperature lower than a temperature required to thermally grow the third oxide layer.

17. The method as recited in claim 14, wherein the depositing of a third oxide layer is carried out such that the third oxide layer has a thickness between about 1200 Angstroms and approximately 1400 Angstroms.

18. The method as recited in claim 14, wherein the removing of a portion of an upper section of the third oxide layer comprises dipping the portion of the upper section in an etchant solution.

19. The method as recited in claim 14, wherein the first and second electrically conductive layers comprise doped polysilicon.

20. The method as recited in claim 14, wherein:
the patterning further comprises patterning the second oxide layer, the first nitride layer, and the first oxide layer, to thereby form the at least one component stack; and
the depositing of a third oxide layer over the at least one component stack is preceded by forming an oxide layer beside the component stack;

21. A semiconductor structure formed using the method set forth in claim 20.

22. A semiconductor structure formed using the method set forth in claim 14.

23. A semiconductor structure formed using the method set forth in claim 16.